



NSREC

**MONDAY, JULY 19, 2010
DENVER, COLORADO**



On behalf of the 2010 Nuclear and Space Radiation Effects Conference (NSREC) Committee, I cordially invite you to attend the 31st annual NSREC Short Course. This four-part course will focus on the design and qualification of integrated circuits and memories for space systems.



Ron Lacoce
SHORT COURSE CHAIRMAN

EACH ATTENDEE WILL RECEIVE A CD-ROM ARCHIVE OF IEEE NSREC SHORT COURSE NOTEBOOKS (1980-2010).

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www.nsrec.com

CUSTOM INTEGRATED CIRCUITS AND MEMORIES: BASIC MECHANISMS, DESIGN AND QUALIFICATION

Announcement for the 2010 NSREC Short Course

COURSE DESCRIPTION

A one-day Short Course "Custom Integrated Circuits and Memories: Basic Mechanisms, Design and Qualification" will be presented at the 2010 Nuclear and Space Radiation Effects Conference (NSREC). With the trend towards increased intrinsic total dose hardness in advanced commercial CMOS processes and the development of hardness-by-design techniques to further mitigate radiation effects as required, many space programs are looking at exploiting commercial CMOS processes for the development of radiation-hardened components for space. The 2010 Short Course will focus on the design and qualification of integrated circuits and memories for space systems.

The Short Course is organized into four sessions starting with a course on developing radiation-hardened system on chip ASICs in advanced commercial CMOS technologies. The second session focuses on microprocessors and static memories for space, while the third session focuses on non-volatile memories for space. The last session discusses assuring reliability and qualification of CMOS components fabricated at commercial CMOS foundries. The speakers for the 2010 Short Course are all experts in their respective areas. They will present the knowledge base in their topical areas with an emphasis on making complex issues understandable to the non-experts, as well as the experts in the field.

The course is applicable to designers, radiation effects engineers, component specialists, and other technical and management personnel who are involved in developing reliable systems designed to operate in space environments. This course provides a unique opportunity for NSREC attendees to benefit from the expertise of the instructors, as well as the in-depth coverage and application-oriented perspective provided by the short course format. The instructors will develop the core content of their respective topics from background material largely found in the literature and from their unique interactions with actual space systems. As such, the course will benefit both new and experienced engineers, scientists, and managers. In-depth notes will be provided at registration.

For those interested in Continuing Education Units (CEUs), there will be an open-book test at the end of the course. The course is valued at 0.6 CEUs and is endorsed by the IEEE and the International Association for Continuing Education and Training (IACET).

Each attendee will receive a complimentary CD-ROM that contains an archive of IEEE Nuclear and Space Radiation Effects Conference (NSREC) Short Course Notebooks (1980-2010). This collection covers 31 years of one-day tutorial courses, presented yearly at NSREC. It serves as a valuable reference for students, engineers, and scientists.

PART I — DEVELOPING RADIATION-HARDENED COMPLEX SYSTEM-ON-CHIP ASICS IN COMMERCIAL ULTRA DEEP SUBMICRON CMOS PROCESSES

Jeremy Popp, Boeing Research and Technology (BR&T), will discuss the challenges and approaches for designing complex radiation-hardened system-on-chip (SoC) ASICs in advanced commercial ultra deep submicron processes. Radiation effect mechanisms in commercial CMOS technologies will be explained, followed by a survey of total ionizing dose and single event effect experimental results in the 90 nm, 65 nm, and 45 nm technology nodes. Radiation hardened by design methodologies (RHBD) covering analysis, simulation, and implementation of complex digital and analog mixed signal circuits will also be presented, including an introductory discussion of RHBD applied to high speed serial-deserializer (SERDES) circuitry. Finally, a discussion of the challenges and approaches to radiation testing of complex SoC designs will be presented.



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PART 2 — MICROPROCESSORS AND SRAMS FOR SPACE: BASICS, RADIATION EFFECTS AND DESIGN

Lawrence T. Clark, Arizona State University, will present a tutorial overview of micro-architecture and circuits for microprocessors at a basic introductory level intended for non-designers. Basic circuit concepts and timing issues will be introduced using examples in the context of a simple embedded microprocessor pipeline. This introduction will lead to an overview of SEE hardening approaches and their impact on design at the micro-architecture (processor pipeline), circuit, and layout level. Since embedded static random access memory (SRAM) comprises up to 90% of microprocessor transistor usage, an introduction to basic SRAM and embedded memory block design will follow, including TID hardening issues. Recent trends towards increased multi-bit upset susceptibility of SRAMs fabricated in advanced CMOS processes will be discussed. Basic memory error detection and correction will then be covered in the context of embedded processor memories. The discussions will be example based and use the simple embedded processor pipeline for perspective throughout.

PART 3 — PRESENT AND FUTURE NON-VOLATILE MEMORIES FOR SPACE

Simone Gerardin and Alessandro Paccagnella, University of Padova, will discuss non-volatile memories (NVMs) for space applications. This talk will first introduce the basic definitions and metrics concerning NVMs, then explore and compare the major storage concepts (floating gate, charge trap, phase change, ferroelectricity, magnetoresistance, nanotubes, etc.), with emphasis on density, performance, reliability, and radiation sensitivity. Architectural information concerning the array organization and peripheral circuitry will be given, highlighting known radiation issues. The focus will be on technologies and devices aimed at the mainstream commercial markets, which, in spite of their issues with ionizing radiation, are very attractive for space designers due to their large size and to small-capacity rad-hard devices. A comprehensive discussion of total dose and single event effects results for this wide cross section of NVMs will be presented.

PART 4 — RELIABILITY AND QUALIFICATION OF CUSTOM INTEGRATED CIRCUITS FOR HARSH ENVIRONMENT APPLICATIONS USING COMMERCIAL WAFER FOUNDRIES

David Kerwin, Aeroflex Colorado Springs, will present a reliability program plan for producing high reliability microelectronics for harsh environments such as space, medical, and nuclear power generation applications. A tutorial on reliability statistics will be given followed by a review of the major physics of failure mechanisms for integrated circuits and packages. A program plan will be presented that considers the entire life cycle (bath-tub curve) of a component. The plan focuses on designing-in and building-in the reliability based upon a detailed reliability assessment of the proposed IC as implemented in a commercial wafer foundry technology. The reliability assessment drives information needed from the foundry before detailed design activities commence. SET/SEU grading of each digital and analog cell in the design allows for error rate to be optimized. The relationship between yield and reliability in terms of optimizing screening methods and monitoring the results of the reliability program plan, including qualification testing, in terms of MIL-PRF-38535 will be discussed. In addition, approaches for qualifying components with respect to radiation effects, including total-ionizing-dose and single-event testing, will be reviewed. A case study of a foundry-portable, radiation-hardened, one-time electrically programmable metal fuse, which demonstrates how the methodology can be used to achieve extremely high reliability by design, concludes the presentation.