Short Course Program

CUSTOM INTEGRATED CIRCUITS AND MEMORIES:
BASIC MECHANISMS, DESIGN AND QUALIFICATION

PLAZA BALLROOMS E, F – MONDAY, JULY 19

7:30 AM	**REGISTRATION/CONTINENTAL BREAKFAST (PLAZA BALLROOMS A, D)**
8:00 AM	**SHORT COURSE INTRODUCTION** Ronald Lacoe *The Aerospace Corporation*
8:15 AM	**PART 1 – DEVELOPING RADIATION-HARDENED COMPLEX SYSTEM-ON-CHIP ASICS IN COMMERCIAL ULTRA DEEP SUBMICRON CMOS PROCESSES** Jeremy Popp *Boeing Research and Technology (BR&T)*
9:45 AM	**BREAK (PLAZA BALLROOMS A, D)**
10:15 AM	**PART 2 – MICROPROCESSORS AND SRAMS FOR SPACE: BASICS, RADIATION EFFECTS AND DESIGN** Lawrence T. Clark *Arizona State University*
11:45 AM	**SHORT COURSE LUNCHEON (PLAZA BALLROOMS A, D)**
1:00 PM	**PART 3 – PRESENT AND FUTURE NON-VOLATILE MEMORIES FOR SPACE** Simone Gerardin and Alessandro Paccagnella *University of Padova*
2:30 PM	**BREAK (PLAZA BALLROOMS A, D)**
3:00 PM	**PART 4 – RELIABILITY AND QUALIFICATION OF CUSTOM INTEGRATED CIRCUITS FOR HARSH ENVIRONMENT APPLICATIONS USING COMMERCIAL WAFER FOUNDRIES** David Kerwin *Aeroflex Colorado Springs*
4:30 PM	**WRAP-UP**
4:40 PM	**EXAM (only for students requesting CEU credit)**
5:10 PM	**END OF SHORT COURSE**

Each attendee will receive a CD-ROM archive of IEEE NSREC Short Course Notebooks (1980-2010).

Short Course

COURSE DESCRIPTION

A one-day Short Course "Custom Integrated Circuits and Memories: Basic Mechanisms, Design and Qualification" will be presented at the 2010 Nuclear and Space Radiation Effects Conference (NSREC). With the trend towards increased intrinsic total dose hardness in advanced commercial CMOS processes and the development of hardness-by-design techniques to further mitigate radiation effects as required, many space programs are looking at exploiting commercial CMOS processes for the development of radiation-hardened components for space. The 2010 Short Course will focus on the design and qualification of integrated circuits and memories for space systems.

The Short Course is organized into four sessions starting with a course on developing radiation-hardened system on chip ASICs in advanced commercial CMOS technologies. The second session focuses on microprocessors and static memories for space, while the third session focuses on non-volatile memories for space. The last session discusses assuring reliability and qualification of CMOS components fabricated at commercial CMOS foundries. The speakers for the 2010 Short Course are all experts in their respective areas. They will present the knowledge base in their topical areas with an emphasis on making complex issues understandable to the non-experts, as well as the experts in the field.

The course is applicable to designers, radiation effects engineers, component specialists, and other technical and management personnel who are involved in developing reliable systems designed to operate in space environments. This course provides a unique opportunity for NSREC attendees to benefit from the expertise of the instructors, as well as the in-depth coverage and application-oriented perspective provided by the short course format. The instructors will develop the core content of their respective topics from background material largely found in the literature and from their unique interactions with actual space systems. As such, the course will benefit both new and experienced engineers, scientists, and managers. In-depth notes will be provided at registration.

For those interested in Continuing Education Units (CEUs), there will be an open-book test at the end of the course. The course is valued at 0.6 CEUs and is endorsed by the IEEE and the International Association for Continuing Education and Training (IACET).

CONTINUING EDUCATION UNITS (CEUS)

Each attendee will receive a complimentary CD-ROM that contains an archive of IEEE Nuclear and Space Radiation Effects Conference (NSREC) Short Course Notebooks (1980-2010). This collection covers 31 years of one-day tutorial courses, presented yearly at NSREC. It serves as a valuable reference for students, engineers, and scientists.

SHORT COURSE CHAIRMAN

Ronald Lacoe
Short Course Chairman

Ronald Lacoe received his B.S., M.S., and Ph.D. in Physics from the University of California, Los Angeles in 1974, 1977, and 1983, respectively. He attended graduate school as a Hughes Aircraft Fellow and worked at the Hughes Research Laboratory in Malibu, California while earning his Ph.D. degree. After receiving his Ph.D., Dr. Lacoe was a joint NSF/CNRS Fellow at the University of Paris-South from 1984-1986, where he worked on reduced-dimensional systems and organic superconductivity. Dr. Lacoe joined The Aerospace Corporation in 1987 as Member of the Technical Staff and is currently a Senior Scientist in the Microelectronics Technology Department, Physical Science Laboratory. Dr. Lacoe has been a pioneer in the development of hardness-by-design methodology as an approach to assuring the supply of high-performance radiation-hardened advanced CMOS components for space missions. In addition, he is also an expert in microelectronic reliability issues for CMOS technologies. He has been responsible for research in the areas of microelectronics reliability and radiation hardness for microelectronics that will be employed in Air Force space programs. Dr. Lacoe has published over one hundred twenty papers, and was the recipient of the 1997 IEEE International Reliability Physics Symposium's Best Paper Award, the 1997 NSREC Meritorious Paper Award and the 1998 NSREC Outstanding Paper Award.

Jeremy D. Popp obtained his BSEE degree from Portland State University, and MEng from UC San Diego. He is currently pursuing his Ph.D. at University of Washington in Electrical Engineering. Jeremy is currently the Mixed Signal ASIC Design Leader at the Boeing Company's Solid State Electronics Development group and manages the research and development of high speed PLL's and SerDes products for space-based applications. Previously, he was a Senior Member of Technical Staff and Lead Circuit Designer at Orora Design Technologies, where he led Orora's PLL IP development in DSM CMOS. He also worked as a program technical leader for the US Navy where he successfully lead several high profile defense electronic system design and advanced technology programs. Jeremy has twelve technical publications, currently holds three patents with several pending, and has received several awards for his exceptional technical accomplishments.

DEVELOPING RADIATION HARDENED COMPLEX SYSTEM-ON-CHIP ASICS IN COMMERCIAL ULTRA DEEP SUBMICRON CMOS PROCESSES

Jeremy Popp
Boeing Research and Technology (BR&T)

Jeremy Popp will discuss radiation effects in commercial ultra deep submicron CMOS technologies, and tools and techniques to solve challenges faced by designers developing complex radiation hardened System on Chip (SoC) designs in these processes. Ongoing research in cutting edge deep submicron CMOS technologies, particularly the 45 nm SOI CMOS node, show significant promise for providing revolutionary improvements in system performance and capabilities while achieving space system radiation hardness requirements. A survey of Total Ionizing Dose and Single Event Effects radiation measurement results will be provided at 90 nm, 65 nm, and 45 nm CMOS technology nodes. Radiation Hardened by Design methodologies (RHBD) covering analysis, simulation, and implementation of complex digital and analog mixed signal circuits will also be presented. This will be followed by a discussion of the challenges and approaches to the radiation testing of complex SoC designs.

Commercial Ultra Deep Submicron Processes

Radiation Hardness Evaluation

- 90 nm and Below
  - TID Hardness of Device Options
  - Representative Heavy Ion and Proton SEU Cross Sections, SET Pulse Generation Rates

Radiation Hardness by Design Techniques

- TID – Layout and Design
- SEE – SEU, SET, SEFI Mitigation

Design Methodologies for Large Scale Digital ASIC's

- Architecture Options (Memory, Control, Processing)
- Clock Distribution Hardening
- Data Path Versus Control Path Options
- EDA Tools Analysis and Design Support

Design Methodologies for Complex Mixed Signal Circuits

- Mitigating TID/SEU/SET Effects in Analog/Mixed Signal Circuits
- EDA Tools Analysis
- Design Examples

Testing Radiation Performance of Complex ASICs

- Facilities for Radiation Testing
- Addressing Test Plans and Technical Challenges
- Test Case of Complex Circuit TID and SEE Testing

Summary

Lawrence T. Clark received the B.S. degree in computer science from Northern Arizona University, in 1984, and the M.S. and Ph.D. degrees in electrical engineering from Arizona State University, in 1987 and 1992, respectively. He worked at Intel in 1982 and from 1984 to 1985, and at VLSI Inc. from 1990 to 1992 performing chipset design. From 1992 to 2003, he worked at Intel in various capacities including microprocessor design (participating in Pentium, Itanium, and XScale processor designs) compact modeling for circuit simulation, and CMOS imager design. Most recently, he was a Principal Engineer and Circuit Design Manager for the XScale Microprocessors for which he received an Intel Achievement Award. In 2003, he joined the Department of Electrical and Computer Engineering, University of New Mexico, Albuquerque, as an Associate Professor. In 2004, Prof. Clark joined the Department of Electrical Engineering at Arizona State University. He has been awarded over 65 patents with approximately 15 pending and has coauthored over 75 peer-reviewed journal and conference articles. Prof. Clark is an associate editor of IEEE TCAS-II and has twice been a guest editor for IEEE Journal of Solid-state Circuits. His research interests are circuits, architectures, and computer-aided design for high-performance and low-power VLSI systems, radiation effects and their mitigation in VLSI systems, and electronics on flexible substrates.

MICROPROCESSORS AND SRAMS FOR SPACE: BASICS, RADIATION EFFECTS AND DESIGN

Lawrence T. Clark
Arizona State University

Lawrence T. Clark will present a tutorial overview of micro-architecture and circuits for microprocessors at a basic introductory level intended for non-designers. Basic circuit concepts and timing issues will be introduced using examples in the context of a simple embedded microprocessor pipeline. This introduction will lead to an overview of SEE hardening approaches and their impact on design at the micro-architecture (processor pipeline), circuit, and layout level. Since embedded static random access memory (SRAM) comprises up to 90% of the transistors in a microprocessor, an introduction to basic SRAM and embedded memory block design will follow, including TID hardening issues. Recent trends towards increased multi-bit upset susceptibility of SRAMs fabricated in advanced CMOS processes will be discussed. Basic memory error detection and correction will then be covered in the context of embedded processor memories. The discussions will be example based and use the simple embedded processor pipeline for perspective throughout.

Introductory Microprocessor Architecture

- Performance Metrics
- Speedup and Amdahl's Law
- A Simple Processor Pipeline
- Pipeline Hazards
- Cache Structure and Operation
- Architectural Versus Speculative State

Sequential Circuits

- Basic Timing and Key Metrics
- Latch and Flip-flop Basics
- Pipeline Timing—Divide and Conquer
- Clocking and Processor Speed

Register File Design

- Circuit Architecture
- Memory Timing

SRAM Design

- Circuit Architecture
- Timing and How SRAM Fits in the Pipeline
- SRAM Variability in Deep Submicron Technologies
- SRAM Cell Stability and Margins
- Sense Amplifiers

Logic Radiation Effects and Mitigation

- Overview
- Mitigation by Process and Design
- Impact of SEE Mitigation on Circuit Timing
- Mitigation Impact on Area and Power

SRAM Radiation Effects and Mitigation

- Mitigation by Process and Design
- TID Mitigation for SRAM Cells
- Mitigation Impact on Area and Power
- SETs in SRAM Periphery Circuits
- Multi-bit Upsets
- Error Detection and Correction

SEE Mitigation Processor Pipeline Impact

- Power and Performance Tradeoffs

Summary

- Looking Forward to Future Technologies

Simone Gerardin received the Laurea degree (cum laude) in Electronics Engineering in 2003, and a Ph.D. in Electronics and Telecommunications Engineering in 2007, both from the University of Padova, Italy. He is currently a research assistant at the same university. His research is focused on soft and hard errors induced by ionizing radiation in advanced CMOS technologies, and on their interplay with device aging and ESD. Simone has authored or co-authored more than 35 papers published in international journals and more than 50 conference presentations, three of which won awards at RADECS 2007, NSREC 2008, and RADECS 2008. In 2005 he received the Phelps Continuing Education Grant from the IEEE Nuclear and Plasma Sciences Society. Simone has been a short course instructor for RADECS 2009.

Alessandro Paccagnella got the Laurea degree in Physics (cum Laude) in 1983 from the University of Padova, Italy. He is now Full Professor of Electronics and Director of the Department of Information Engineering at the University of Padova. He is the author of more than 300 scientific papers, and about 200 of them have been published on international journals. In the past, his research activity has been directed to the study of different aspects of physics, technology, and reliability of semiconductor devices. At present, he coordinates the activity of a research group focused on the study of ultra-thin gate dielectrics in MOS devices and on Total Ionizing Dose and Single Event Effects induced by ionizing radiation on integrated circuits, with emphasis on non-volatile memories and programmable logic devices. He has co-authored works, which received Awards at the conferences ESREF 92, ESREF 98, NSREC 1999, ESSDERC 2000, RADECS 2007, NSREC 2008 and RADECS 2008.

PRESENT AND FUTURE NON-VOLATILE MEMORIES FOR SPACE

Simone Gerardin and Alessandro Paccagnella
University of Padova

Simone Gerardin and Alessandro Paccagnella will discuss non-volatile memories (NVMs) for space applications. This talk will first introduce the basic definitions and metrics concerning NVMs, then explore and compare the major storage concepts (floating gate, charge trap, phase change, ferroelectricity, magnetoresistance, nanotubes, etc.), with emphasis on density, performance, reliability, and radiation sensitivity. Architectural information concerning the array organization and peripheral circuitry will be given, highlighting known radiation issues. The focus will be not only on technologies and devices aimed at the mainstream commercial markets, which, in spite of their issues with ionizing radiation, are very attractive for space designers due to their large size, but also on small-capacity rad-hard devices. A comprehensive discussion of total dose and single event effects results for this wide cross section of NVMs will be presented.

Overview and Basics
- Endurance and Retention
- Non-Volatile Storage Concepts
- Array Architecture and Peripheral Circuitry
- Commercial Market Versus Space Market

Charge-based Technologies
- Floating Gate Architecture
- Array Organization
- Peripheral Circuitry
- Radiation Effects
- Scaling
- Nanocrystal Cells
- Charge-Trap Cells

Phase Change Memories
- Chalcogenide Materials
- Reliability And Radiation Effects

Ferroelectric Memories
- Remnant Polarization
- Reliability And Radiation Effects

Magnetoresistive Memories
- Principles Of Operation
- Reliability And Radiation Effects

Comparison and Prospects
- Universal Memory?

Future Technologies
- Carbon Nanotube Memories
- Resistive Random Access Memories
- Miscellaneous

Conclusions

David Kerwin received a B.S. in Chemistry from the University of Notre Dame in 1979, an M.S. in Physics from Colorado State University (CSU) in 1985, and performed Ph.D. research at CSU in the area of "Radiation-Induced, Paramagnetic Defects in amorphous Silicon Dioxide." He has been with Aeroflex Colorado Springs (formerly UTMC) since 1984, where he has held various technical and management positions, and is currently the Director of Mixed-Signal Products, a team designing full-custom integrated circuits that interface to sensors used in harsh environments. He has worked with commercial wafer foundries for high-reliability microelectronics for the past 14 years. He has earned American Society for Quality (ASQ) certifications in Reliability Engineering, Quality Engineering, and Quality Auditing. He has authored over 20 technical articles in publications such as Physical Review Letters, Physical Review B, Journal of Applied Physics, and IEEE Radiation Effects Data Workshop. He has been awarded seven patents in the areas of radiation hardening of CMOS processes and x-ray detectors.

RELIABILITY AND QUALIFICATION OF CUSTOM INTEGRATED CIRCUITS FOR HARSH ENVIRONMENT APPLICATIONS USING COMMERCIAL WAFER FOUNDRIES

David Kerwin
Aeroflex Colorado Springs

David Kerwin will present a reliability program plan for producing high reliability microelectronics for harsh environments such as space, medical, and nuclear power generation applications. A tutorial on reliability statistics will be given followed by a review of the major physics of failure mechanisms for integrated circuits and packages. A program plan will be presented that considers the entire life cycle (bath-tub curve) of a component. The plan focuses on designing-in and building-in the reliability based upon a detailed reliability assessment of the proposed IC as implemented in a commercial wafer foundry technology. The reliability assessment drives information needed from the foundry before detailed design activities commences. SET/SEU grading of each digital and analog cell in the design allows for error rate to be optimized. The relationship between yield and reliability in terms of optimizing screening methods and monitoring the results of the reliability program plan, including qualification testing, in terms of MIL-PRF-38535 will be discussed. In addition, approaches for qualifying components with respect to radiation effects, including total-ionizing-dose and single-event testing, will be reviewed. A case study of a foundry-portable, radiation-hardened, one-time electrically programmable metal fuse, which demonstrates how the methodology can be used to achieve extremely high reliability by design, concludes the presentation.

Introduction To Reliability
- Definition of Reliability
- Probability Distributions
- Reliability Equations
- The Bathtub Curve
- System Reliability

Planning For Reliability
- The Reliability "Plan-Do-Check-Act" Cycle
- Reliability Program Plan

Designing-In Reliability
- Reliability Model for an Integrated Circuit
- Physics of Failure: Intrinsic Failure Mechanisms
- Physics of Failure: Extrinsic Failure Mechanisms
- Hermetic Package Reliability
- Reliability Assessment based upon Foundry Data

Building-In Reliability
- Intrinsic Versus Extrinsic Reliability
- Process Controls and SPC
- Testing and Fault Coverage
- Yield and Reliability
- Value-Added Screening

Monitoring Reliability
- Qualification and Hardness Assurance Testing
- Periodic Reliability Testing
- Long Term Reliability Testing

Improving Reliability
- Failure Analysis
- Corrective Action System
- Continuous Process Improvement

Summary