Challenges and Opportunities for Radiation Hardening in Advanced Technologies

Announcement for the 2021 IEEE NSREC Short Course

MONDAY
JULY 19, 2021
OTTAWA,
CANADA

On behalf of the 2021 IEEE Nuclear and Space Radiation Effects Conference (NSREC) Committee, I cordially invite you to attend the 42nd IEEE NSREC Short Course. An outstanding group of technical experts will provide an in-depth discussion of the hardening techniques at device, circuit, and system level needed to cope with the threat of ionizing radiation.

Dr. Marta Bagatin
University of Padova, Dept. of Information Engineering
Short Course Chair

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COURSE DESCRIPTION

A short course, *"Challenges and Opportunities for Radiation Hardening in Advanced Technologies"*, will be presented at the 2021 IEEE Nuclear and Space Radiation Effects Conference. Semiconductor technology evolution has led to circuits that are more vulnerable to some radiation effects, while mitigating others. Choosing the most suitable technique to harden electronics against radiation and finding the right tradeoff between protection and performance penalty, is crucial to design effective and reliable space or safety-critical systems.

The short course is organized into four sections, all featuring introductory material and advanced topics, with an emphasis on radiation hardening. The first section addresses hardening for digital circuits, with emphasis on single-event effects, spanning from traditional techniques to recent developments in novel technologies. The second part focuses on hardening for analog and mixed-signal circuits, discussing layout and circuit-level approaches for the mitigation of single-event and total ionizing dose effects. The third section illustrates hardening in imagers, but includes solutions applicable to other ASICs: it is centered on total dose effects mitigation and briefly covers also ultra-high-dose applications. The final course deals with system-level approaches, providing case studies, lessons learnt, and solutions for the use of commercial components in spacecraft electronics. More detailed descriptions of each lecture are provided below. The topics covered should benefit people new to the field as well as experienced engineers and scientists, by providing up-to-date material and insights.

The short course is intended for radiation effects engineers, component specialists, system designers, and other technical and management personnel involved in developing reliable systems designed to operate in radiation environments. It provides a unique opportunity for IEEE NSREC attendees to benefit from the expertise of excellent instructors, along with a critical review of state-of-the-art knowledge in the field. Electronic copies of detailed course notes will be provided to each participant.

Continuing Education Units (CEUs) will be available. For the interested attendees, an exam will be given at the end of the short course. The course is valued at 0.6 CEUs, and is endorsed by the IEEE and by the International Association for Continuing Education and Training (IACET).

PART I – HARDENING TECHNIQUES FOR DIGITAL CIRCUITS

Dr. Balaji Narasimham, Broadcom, will provide an overview of the single-event effects in digital circuits and discuss traditional to current techniques in radiation-hardening and radiation-tolerant designs. The semiconductor industry has been striving to keep up with Moore's law scaling predictions through innovative process solutions from planar to current FinFET processes. This has helped develop high-performance application specific integrated circuits (ASIC) to suit a variety of space and terrestrial applications. On the other hand, with technology scaling and the associated increase in packing densities and reduction in operating voltages, the critical charge needed to cause single-event effects in digital circuits has decreased significantly resulting in increased vulnerability to radiation. This short course will review hardening-by-design approaches used for overcoming single-events in memories, latches and logic circuits. Error correction techniques for memories along with spacial- and time- redundancy based approaches for latches and logic circuits will be presented. Recent advancement in the radiation-tolerant design approaches that tradeoff performance penalty with the extent of radiation tolerance to suit different applications will be discussed along with the performance overhead vs. radiation tolerance comparisons. Finally, the course will review scaling trends and bias dependence of single-event upset rates from planar to FinFET processes with an emphasis on the opportunities and challenges for radiation hardening in highly scaled technologies.

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PART II – HARDENING TECHNIQUES FOR ANALOG AND MIXED-SIGNAL CIRCUITS

Dr. Daniel Loveless, University of Tennessee at Chattanooga, will present an overview of basic and state-of-the-art approaches for the mitigation of radiation effects in analog and mixed-signal (analog + digital) circuits. The hardening of such components is typically thought to require a "brute force" approach; that is, area and power are often sacrificed through the increase of capacitance, device size, and current drive. Moreover, there are no standard metrics for radiation effects in analog and mixed-signal circuits as the responses are dependent on the circuit topology, implementation, operating mode, and technology. This presentation addresses these challenges by classifying various techniques based on a few underlying principles and illustrates how these mitigation principles can be manifest in topology-specific examples. Part 1 of the presentation will discuss mitigation strategies that are generally focused on either increasing the critical charge to upset or on reducing the amount of collected charge at metallurgical junctions. Part 2 continues by providing examples of hardened circuits, and catalogues the techniques based on the underlying mitigation principles. The primary focus of the presentation will be on layout and circuit-level approaches to the mitigation of single event effects and total ionizing dose.

PART III – HARDENING TECHNIQUES FOR IMAGE SENSORS

Dr. Vincent Goiffon, ISAE-SUPAERO, University of Toulouse, will provide an overview of the main radiation-induced degradations in solid state image sensors and present mitigation techniques to improve their radiation hardness and enable their use in harsh radiation environments. Among the wide variety of radiation effects relevant for pixel arrays and detectors, radiation-induced leakage currents in PN junctions are by far the main factor limiting the performances of these mixed signal integrated circuits when exposed to fields of high energy particles. How Total Ionizing Dose affects these leakages and how design and process optimizations can reduce the dark current in irradiated sensors will be discussed. What can enhance or reduce the sensitivity of an image sensor to more specific effects such as displacement damage and radiation induced random telegraph signal will also be addressed. The presentation will primarily focus on the CMOS Image Sensor technology, but will also explore the applicability of the presented concepts to other solid state image sensor technologies, as well as the similarities with other leakage sensitive devices such as DRAMs. This presentation will conclude by an overview of the relevant pixel radiation hardening techniques to use depending on the application requirements: from Earth observation space instruments to the exploration of the Jovian system and nuclear fusion instrumentation.

PART IV – SYSTEM-LEVEL HARDENING - WHAT COULD GO WRONG, AND HOW TO MAKE IT RIGHT

Kay Chesnut, Engineering Fellow, Radiation Effects Engineering, Raytheon Intelligence & Space at Raytheon Technologies will briefly review historical space failures, known root causes, and the resulting requirements that drive system mitigation strategies for use of commercial components in spacecraft electronics. The talk, "What Could Go Wrong, and How To Make It Right" will tackle system level hardening strategies by looking at the main components of space systems, the applicable radiation environments that particularly plague those components, and the design approaches used to work around those radiation impacts. Examples will be pulled from the public domain to illustrate the techniques. Emphasis will be on work done in flexible platforms brought online using re-programmable FPGAs as an illustration of some of the system considerations.